Reg. No. | | | | | | | | | | |

Q.P. Code:16EC5507 **R16**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester (R16) Regular Examinations May/June 2017

TESTING & TESTABILITY

(Common to ES & VLSI)

(For Students admitted in 2016 only)

Time: 3 hours Max. Marks:60

(Answer all Five Units 5 X 12 =60 Marks)

UNIT-I

1	a.	Explain about controlling value and inversion value for a combinational circuit. Discuss how the gate evaluation is carried out by input scanning	6M
	b.	What are the different functional modeling techniques at the logic level? Explain about any two techniques.	6M

OR

2	a.	Explain the logic simulation of applications	6M
	b.	What is meant by hazards? Mention its types and how they are detected.	6M

UNIT-II

3	a.	Describe the source of fault mechanism.How the fault can be detected and located.	6M
	b.	Write a short note on fault modes.	6M

OR

4	a.	Explain about multiple stuck-fault models.	6M
	b.	Given some of the applications of fault simulation.	6M

UNIT-III

5	a.	Differentiate between board level and system level DFT approaches	6M
	b.	Explain the Generic Boundary Scan	6M

OR

6	a.	How to perform syndrome test and signature analysis in digital circuits	6M
	b.	Explain about board level and system level DFT approaches	6M

UNIT-IV

7	a.	Discuss the different errors/faults that are associated with memory operation	6M
	b.	Explain any two BIST concepts	6M

OR

8	a.	Explain design for self-test at board level	6M
	b.	Explain BIST architectures of LOCST,RTD	6M

UNIT-V

9	a.	Explain any two types of memories and Integration	6M
	b.	What is meant by embedded core testing ?Explain	6M

OR

10	a.	Explain about the memory test requirements for MBIST	6M
	b.	Write down the important features of JTAG testing.	6M

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